WHAT IS CLAIMED IS:

1. A switching circuit device comprising:

a first set of filed effect transistors connected in series;

a second set of filed effect transistors connected in series;

a common input terminal connected to a source electrode or a drain electrode of a transistor positioned at one end of the first set and connected to a source electrode or a drain electrode of a transistor positioned at one end of the second set;

a first output terminal connected to a source electrode or a drain electrode of a transistor positioned at other end of the first set;

a second output terminal connected to a source electrode or a drain electrode of a transistor positioned at other end of the second set;

a first control terminal connected to gate electrodes of all the transistors of the first set;

a second control terminal connected to gate electrodes of all the transistors of the second set; and

a protecting element comprising an insulating region disposed between two high impurity concentration regions,

wherein the protecting element is connected between the source or drain electrode of the transistor positioned at the one end of the first set and the gate electrode of the transistor positioned at the one end of the first set, between the source or drain electrode of the transistor positioned at the one end of the second set and the gate electrode of the transistor positioned at the one end of the second set, between the source or drain electrode of the transistor connected to the first output terminal and the gate electrode of the transistor connected to the first output terminal, or between the source or drain electrode of the transistor connected to the second output terminal and the gate electrode of the transistor connected to the second output terminal.

2. A switching circuit device comprising:

a first set of filed effect transistors connected in series and formed on a chip;

a second set of filed effect transistors connected in series and formed on the chip;

a common input terminal connected to a source electrode or a drain electrode of a transistor positioned at one end of the first set and connected to a source electrode or a drain

electrode of a transistor positioned at one end of the second set;

a first output terminal connected to a source electrode or a drain electrode of a transistor positioned at other end of the first set;

a second output terminal connected to a source electrode or a drain electrode of a transistor positioned at other end of the second set;

a first control terminal connected to gate electrodes of all the transistors of the first set;

a second control terminal connected to gate electrodes of all the transistors of the second set;

a plurality of electrode pads formed on the chip, each of the electrodes pads being connected to one of the terminals; and

a high impurity concentration region formed at a periphery of each of the electrode pads,

wherein the electrode pad connected to the common input terminal and the electrode pad connected to a gate electrode of the transistor positioned at the one end of the first or second set are disposed at both sides of and adjacent a narrow insulating region, or the electrode pad connected to the first or second output terminal and the electrode pad connected to a gate electrode of a corresponding transistor positioned at the other end of the first or second set are disposed at both sides of and adjacent another narrow insulating region.

3. The switching circuit device of claim 2, wherein the electrode pad connected to the common input terminal and the electrode pad connected to the gate electrode of the transistor positioned at the one end of the first set are disposed at both sides of and adjacent one of the narrow insulating regions, the electrode pad connected to the common input terminal and the electrode pad connected to the gate electrode of the transistor positioned at the one end of the second set are disposed at both sides of and adjacent one of the narrow insulating regions, the electrode pad connected to the first output terminal and the electrode pad connected to the gate electrode of the corresponding transistor positioned at the other end of the first set are disposed at both sides of and adjacent one of the narrow insulating regions, and the electrode pad connected to the second output terminal and the electrode pad connected to the gate electrode of the corresponding transistor positioned at the other end of the second set are disposed at both sides of and adjacent one of the narrow insulating regions.

4. The switching circuit device of claim 2, further comprising a plurality of additional electrode pads that are connected to a gate electrode, a source electrode or a drain electrode of the transistors that not connected to the terminals, the additional electrode pads being connected to inspection terminals.

5. The switching circuit device of claim 2, further comprising:

an insulating substrate, the chip being bonded to a front surface of the insulating substrate;

external electrodes disposed on a rear surface of the insulating substrate, each of the external electrodes being provided for one of the terminals;

a plurality of conductive leads disposed on the front surface of the insulating substrate, each of the conductive leads being connected to one of the external electrodes and one of the electrode pads; and

a resin layer covering the chip and insulating substrate.

6. The switching circuit device of claim 3, further comprising:

an insulating substrate, the chip being bonded to a front surface of the insulating substrate;

external electrodes disposed on a rear surface of the insulating substrate, each of the external electrodes being provided for one of the terminals;

a plurality of conductive leads disposed on the front surface of the insulating substrate, each of the conductive leads being connected to one of the external electrodes and one of the electrode pads; and

a resin layer covering the chip and insulating substrate.

7. The switching circuit device of claim 6, wherein all the gate electrodes of the transistors of the first set are connected to one of the conductive leads through corresponding electrode pads, and all the gate electrodes of the transistors of the second set are connected to another of the conductive leads through corresponding electrode pads.

8. The switching circuit device of claim 4, further comprising:

an insulating substrate, the chip being bonded to a front surface of the insulating substrate;

external electrodes disposed on a rear surface of the insulating substrate, each of the external electrodes being provided for one of the terminals;

a plurality of conductive leads disposed on the front surface of the insulating substrate, each of the conductive leads being connected to one of the external electrodes and one of the electrode pads; and

a resin layer covering the chip and insulating substrate.

9. The switching circuit device of claim 8, wherein the external electrodes connected to the inspection terminals are smaller than the external electrodes connected to the terminals that are not the inspection terminals.

10. A switching circuit device comprising:

a series of filed effect transistors formed on a substrate and connected in series;

an input electrode pad disposed on the substrate and connected to a source electrode or a drain electrode of a transistor positioned at one end of the series;

an output electrode pad disposed on the substrate and connected to a source electrode or a drain electrode of a transistor positioned at other end of the series;

a first control electrode pad disposed on the substrate and connected to a gate electrode of the transistor at the one end of the series;

a second control electrode pad disposed on the substrate and connected to a gate electrode of the transistor at the other end of the series; the second control electrode pad being connected to the first control electrode pad;

a high impurity concentration region formed in the substrate and at a peripheral portion of each of the electrode pads;

wherein the input electrode pad and the first control electrode pad are disposed so that the high impurity concentration regions of the input electrode pad and the first control electrode pad face each other and are separated by a first thin portion of the substrate, or the output electrode pad and the second control electrode pad are disposed so that the high impurity concentration regions of the output electrode pad and the second control electrode pad face each other and are

separated by a second thin portion of the substrate.

11. The switching circuit device of claim 10, wherein a thickness of the first thin portion or the second thin portion is 5 μm or smaller.

12. The switching circuit device of claim 10, wherein a thickness of the first thin portion or the second thin portion is such that a protecting element is formed between the corresponding high impurity concentration regions.